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SHALLOW TRENCH ISOLATION AND FABRICATING METHOD THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a semiconductor device structure and fabricating method thereof. More particularly, the present invention relates to a shallow trench isolation and fabricating method thereof.

Description of the Related Art

[0002] With the rapid development of integrate circuits, device miniaturization for higher integration is a major trend. As the dimension of each device is reduced and the level of integration is increased, the dimension of the isolation structures between devices must be reduced as well. In other words, more sophisticated techniques for isolating devices must be used as distance of separation between devices is reduced. At present, shallow trench isolation is often used in the fabrication of sub-half micron or smaller integrated circuits.

[0003] To produce a shallow trench isolation (STI) structure, a trench is formed in a semiconductor substrate. Thereafter, an oxide material is deposited into the trench serving as an isolation layer. Since the STI structure has the advantage of easy size adjustment but without the disadvantage of the bird's beak encroachment problem as in the

case of a conventional local oxidation (LOCOS) isolation technique, and therefore ideal for fabricating sub-half micron or smaller metal-oxide-semiconductor (MOS).

[0004] The earlier version of the STI structure is fabricated simply by filling a substrate trench with an insulating material. However, due to the presence of residual stress around the peripheral substrate, dislocation of the lattice is common. This lattice dislocation is often the cause of current leakage. One common method of relieving residual stress is to form a silicon nitride liner between the trench surface and the layer of insulating material.

[0005] In general, the silicon nitride liner in a STI structure has a thickness greater than 120Å. Hence, for a narrow trench having a width of 0.13μm or smaller, the trench aspect ratio will increase considerably and the subsequent deposition of insulating material into the trench will be difficult. Furthermore, a few silicon nitride particles may be retained on the wafer after the formation of the liner. Since these silicon nitride particles have considerable adverse effects on the quality of the wafer, silicon nitride liner is no longer formed on a trench with a width of 0.13μm or smaller. Yet, without the silicon nitride liner, residual stress problem persists.

[0006] An alternative method of reducing residual stress around the trench is to increase the temperature during the densification of the insulating material so that the peripheral lattice is realigned to relieve stress and reduce the number of dislocations. However, the densification temperature must not be too high (or processed too long) to prevent dopant diffusion. Ultimately, the degree of residual stress relaxation is quite limited.

SUMMARY OF THE INVENTION

[0007] Accordingly, one object of the present invention is to provide a shallow trench isolation (STI) structure and fabricating method thereof capable of relieving residual stress around the trench region to eliminate possible effects on subsequent processing operations.

[0008] A second object of this invention is to provide a shallow trench isolation (STI) structure and fabricating method thereof capable of relieving residual stress around the trench region with very little or negligible impact on the trench aspect ratio.

[0009] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of fabricating a shallow trench isolation structure. First, a substrate is provided. A patterned mask layer is formed over the substrate. Using the mask layer as an etching mask, the substrate is patterned to form a trench. Thereafter, a nitridation process is performed to form a silicon nitride liner on the surface of the trench. The nitridation process comprises a furnace treatment, a rapid thermal treatment or a plasma treatment. Finally, an insulating material is deposited to fill the trench.

[0010] Because the thickness of the silicon nitride liner formed by a nitridation process is very small (50Å to 60Å), the silicon nitride liner has very little or negligible impact on the trench aspect ratio. In other words, the silicon nitride liner is capable of relieving residual stress on the peripheral region of the substrate, and the insulating material can be easily filled into the trench in the subsequent process.

[0011] This invention also provides a shallow trench isolation (STI) structure. The STI structure comprises a substrate, a silicon nitride liner and an insulation layer. The substrate has a trench and the silicon nitride liner is formed on the surface of the trench. The silicon nitride liner has a thickness between 50Å to 60Å. Furthermore, the insulation layer completely fills the trench so that the insulation layer and the surface of the trench are separated from each other by the silicon nitride liner.

[0012] Since the thickness of the silicon nitride liner between the trench surface and the insulation layer of the STI structure is smaller than the conventional liner (>120Å), its impact on the trench aspect ratio is small or negligible. Hence, the process of filling the trench with an insulating material can be carried out with ease.

[0013] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0015] Fig. 1 is a flow chart showing the steps for fabricating a shallow trench isolation structure according to one preferred embodiment of this invention.

[0016] Figs. 2A through 2E are schematic cross-sectional views showing the progression of process steps for fabricating the STI structure in Fig. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0018] Fig. 1 is a flow chart showing the steps for fabricating a STI structure according to one preferred embodiment of this invention. Figs. 2A through 2E are schematic cross-sectional views showing the progression of process steps for fabricating the STI structure in Fig. 1. As shown in Figs. 1 and 2A, a substrate is provided (step 100). A patterned mask layer 204 is formed over the substrate 200 (step 102). The patterned mask layer 204 has an opening that exposes a portion of the substrate 200. The mask layer 204 is a silicon nitride layer formed, for example, by depositing mask material over the substrate 200 globally to form a mask layer (not shown). Thereafter, a patterned photoresist layer is formed over the mask layer and the mask layer is patterned using the patterned photoresist layer. After patterning the mask layer, the patterned photoresist layer is removed.

[0019] In addition, a pad oxide layer 202 may also be formed over the substrate 200 before forming the global mask layer to lower the stress between the substrate 200 and the mask layer 204. The pad oxide layer 202 is also patterned in the subsequent patterning

process of the mask layer 204. The pad oxide layer 202 is formed, for example, by performing a thermal oxidation process.

[0020] As shown in Figs. 1 and 2B, the substrate 200 is etched using the mask layer 204 as an etching mask to form a trench 206 (step 104). The etching process includes an anisotropic dry etching operation, for example.

[0021] As shown in Figs. 1 and 2C, a nitridation process 106 is performed to form a silicon nitride liner 212 with a thickness between 50Å to 60Å on the surface of the trench 206. The nitridation process 106 can be comprised of a furnace treatment, a rapid thermal treatment or a plasma treatment, for example. The furnace treatment or the rapid thermal treatment is carried out in an atmosphere of gaseous nitrogen and the plasma treatment is carried out using nitrogen plasma.

[0022] It is to be noted that the silicon nitride liner 212 produced by the nitridation process 106 is very thin. Accordingly, the silicon nitride liner layer 212 will have negligible impact on the trench 206 aspect ratio. In other words, an insulating material can be deposited to fill the trench (in step 108) without much difficulties. Furthermore, because the silicon nitride liner 212 is directly formed on the surface of the trench 206 in a nitridation process 106, the problem of wafer contamination by silicon nitride particles will not occur. In addition, the nitridation process 106 may also be integrated with the fabrication of the liner oxide layer. For doing so, all one need to do is adding some gaseous nitrogen to the thermal oxidation process for forming the liner oxide layer 210 on the surface of the trench 206. In fact, the silicon nitride liner 212 is formed in-situ over the liner oxide layer 210.

[0023] As shown in Fig. 1 and 2D, an insulation layer 214 is formed over the substrate 200 completely filling the trench (step 108). The insulation layer 214 is a silicon oxide layer and can be formed, for example, by performing a high-density plasma chemical vapor deposition (HDPCVD) process. Since the silicon nitride liner 212 formed in step 106 is relatively thin, its impact on the trench 206 aspect ratio is minimal. In other words, the silicon nitride liner 212 has very little negligible impact on the filling of the trench 202 with an insulating material 214 in step 108.

[0024] As shown in Fig. 2E, the insulation layer 214 outside the trench 206 is removed by performing chemical-mechanical polishing (CMP) operation. Consequently, only the insulation layer 214a is retained inside the trench 206. Finally, the pad oxide layer 202 on the substrate 200 and the mask layer 204 are removed. Thus, the process of fabricating a shallow trench isolation (STI) structure is completed.

[0025] In summary, the nitridation process according to this invention is capable of producing a thin silicon nitride liner. The silicon nitride liner of the present invention has very little or negligible impact on the trench aspect ratio, and therefore the insulating material can be easily filled into the trench for fabricating highly integrated circuits. Furthermore, because the nitridation treatment is directly carried out on the trench surface, therefore the problem of silicon nitride particles contaminating the wafer as in case of the conventional process as described above can be effectively resolved.

[0026] As shown in Fig. 2E, a shallow trench isolation (STI) structure according to this invention comprises a substrate 200, a silicon nitride liner 212 and an insulation layer 214a. The substrate 200 comprises a trench 206. The silicon nitride liner 212 is formed

on the surface of the trench 206. The silicon nitride liner 212 has a thickness in a range of about 50Å to 60Å. The insulation layer 214a fills the trench 206 completely. The insulation layer 214a is comprised of a silicon oxide layer, for example. The STI structure furthermore comprises a liner oxide layer 210 set between the surface of the trench 206 and the silicon nitride liner 212.

[0027] Accordingly, the silicon nitride liner between the surface of the trench and the insulation layer has a thickness smaller than the silicon nitride layer in a conventional STI structure. Therefore, the silicon nitride liner of the present invention will have a very little or negligible impact on the trench aspect ratio so that the trench can be reliably filled during the trench-filling process. In the meantime, the silicon nitride liner of the present invention within the STI structure is capable of relieving the residual stress around the peripheral region of the substrate, and thus the reliability of the semiconductor device can be effectively promoted.

[0028] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.